

# DFI Lanparty JR P45-T2R

## BIOS Setting Guideline

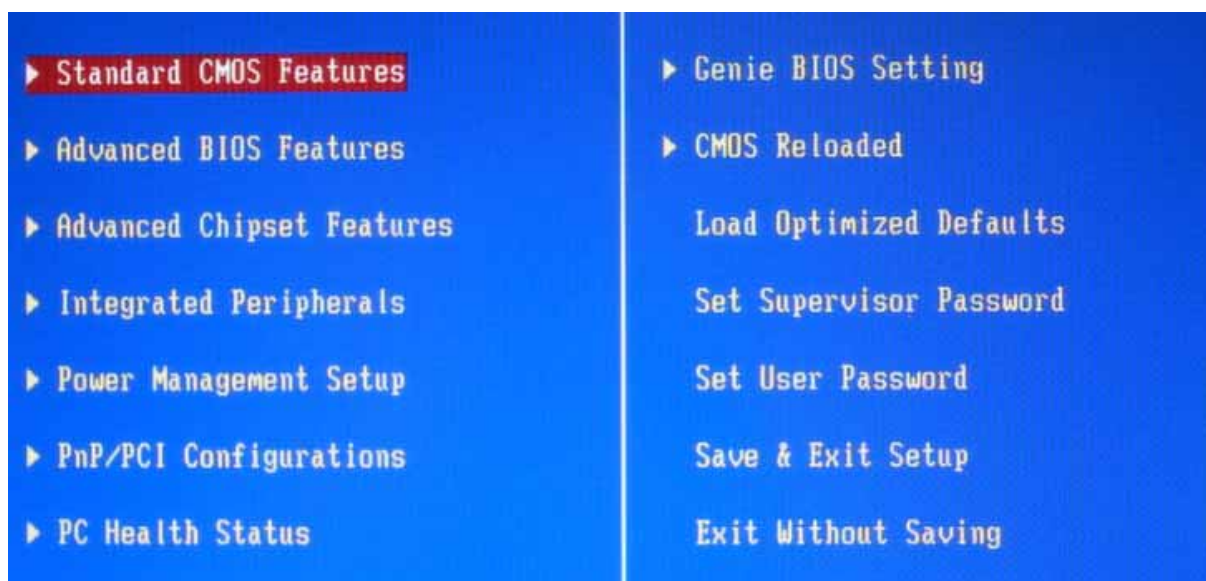
(BIOS version: 2008/08/12) V001

- Pressing **DEL** at DFI JR P45-T2R / Plus logo screen to login BIOS setup screen

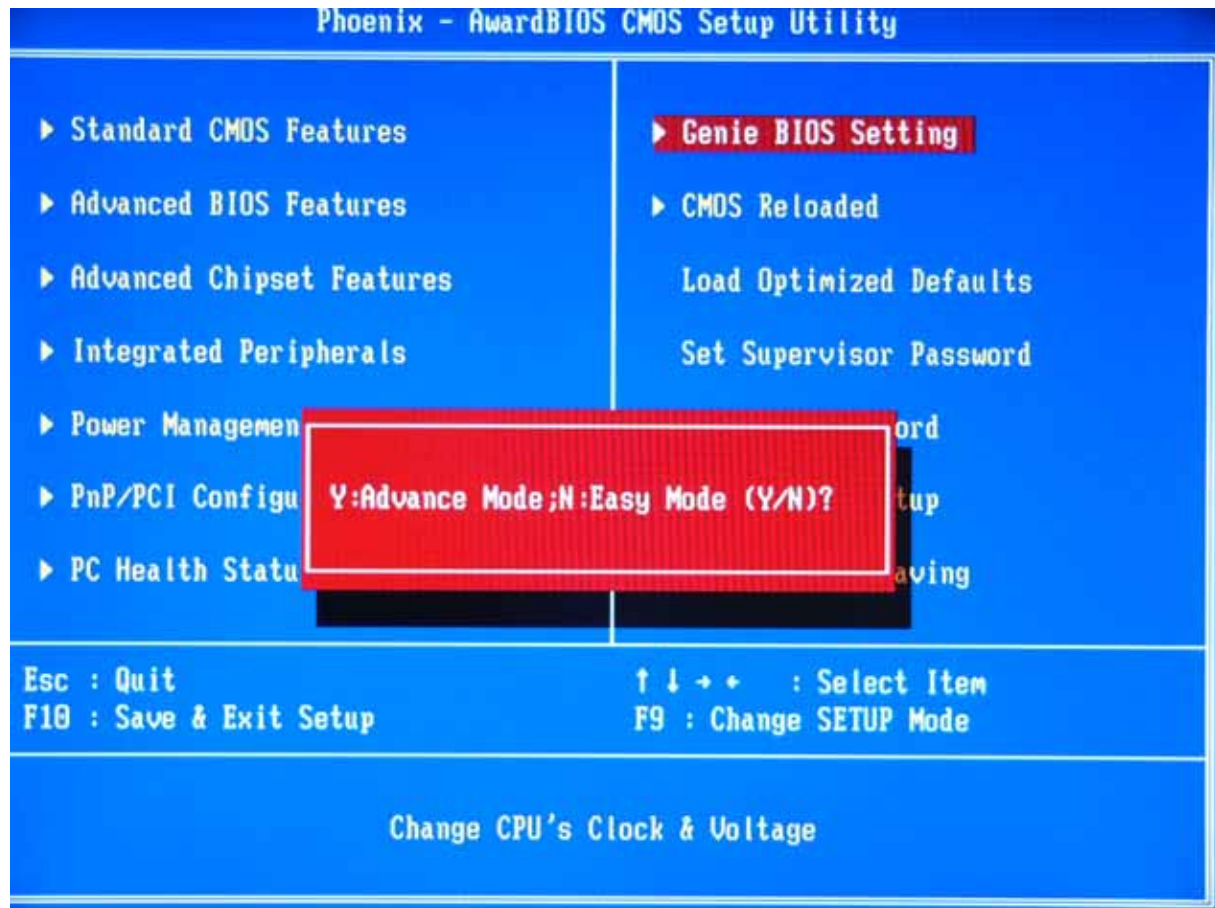


- BIOS setup screen

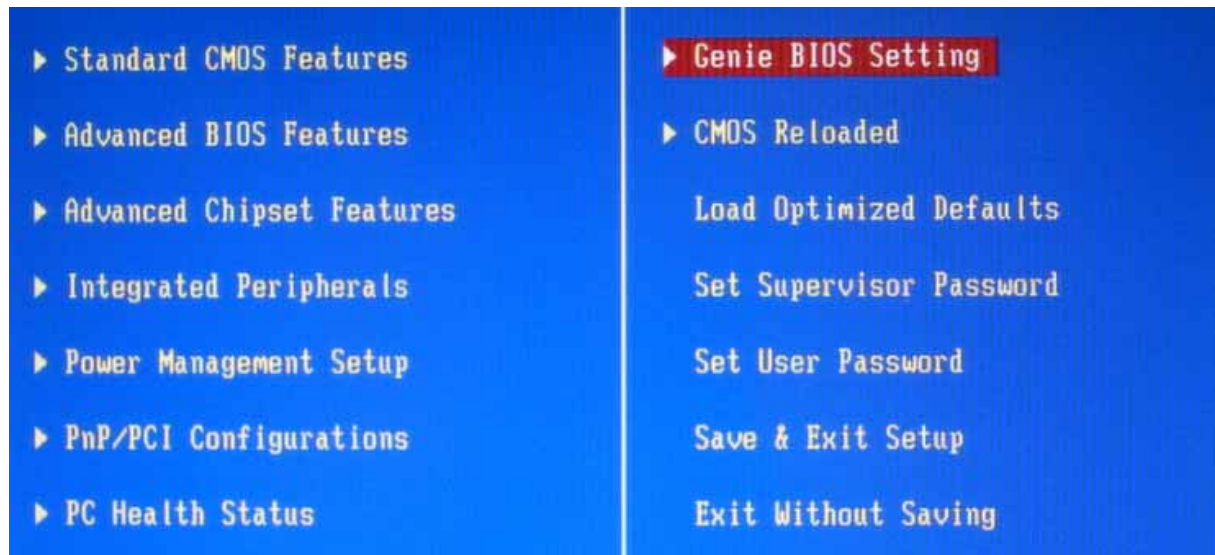
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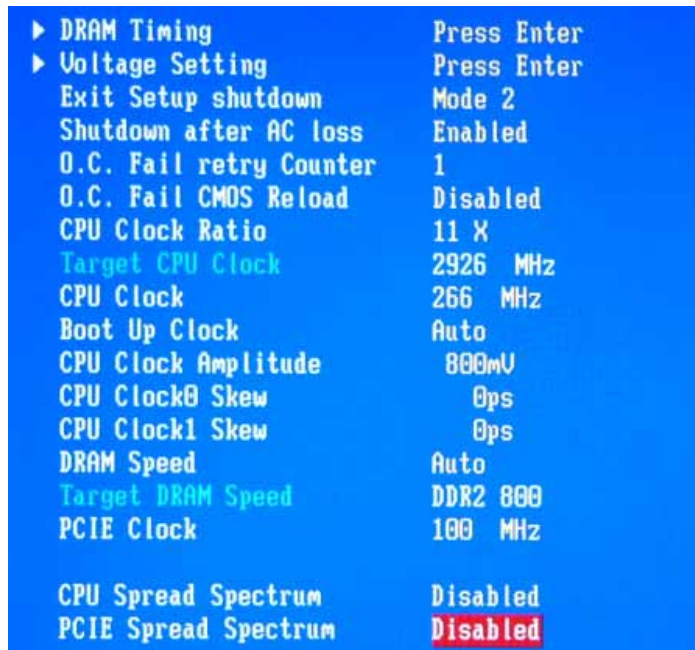
- Advance BIOS mode: Press **F9** at main setup screen to swap to **advance mode**



- Genie BIOS settings: This setup thread is combined all needed settings for over clocking (CPU speed setting, CPU features, DRAM timings, Voltage settings and PCI speed etc.)



➤ Genie BIOS : *Main setup screen*



▶ DRAM Timing	Press Enter
▶ Voltage Setting	Press Enter
Exit Setup shutdown	Mode 2
Shutdown after AC loss	Enabled
O.C. Fail retry Counter	1
O.C. Fail CMOS Reload	Disabled
CPU Clock Ratio	11 X
Target CPU Clock	2926 MHz
CPU Clock	266 MHz
Boot Up Clock	Auto
CPU Clock Amplitude	800mV
CPU Clock0 Skew	0ps
CPU Clock1 Skew	0ps
DRAM Speed	Auto
Target DRAM Speed	DDR2 800
PCIE Clock	100 MHz
CPU Spread Spectrum	Disabled
PCIE Spread Spectrum	Disabled

**Exist Setup Shutdown: Mode1/Mode2**

Somehow it's a "characteristic" of Intel chipset when overclocking... it will shutdown after tweaking. For that, DFI has 2 different modes to chose:

**Mode 1)** when the system was boot-up, it will run a little "diagnose".

If the CPU frequency doesn't change too much, it will skip the "shutdown" function and rewrite the clock generator directly.

**Mode 2)** no matter how little the CPU clock or DRAM's ratio has been changed,

The system still "shutdown" and reboot by itself

**Shutdown after AC Loss: Enable/Disable**

System Power recovers item. (Enabled for power on system automatically if AC power failure)

**OC Fail Retry Counter: 0~3 times**

OC fail retry looping setting. For example, set it on 1, it will retry boot again if fail, then **auto back CPU default** value to boot system.

**OC Fail CMOS reload: Disable / Bank1~3**

Assign bank settings reload for boot when OC fail

**CPU Clock ratio:**

CPU multiplier setting, **6~11** for locked processors, **6~50** times for unlocked processors

### CPU Clock range:



### Boot-up clock: Auto/ 200MHz ~510MHz

This function can help you out for setting a lower boot up clock. As a buffer, when your FSB is tweaked too high in the beginning. The process will be: system boot up with “Boot-up clock” first, after that it will change to your highest FSB.

### CPU Clock Amplitude :

Clock output strength, to add it for increasing grow weaker signal to terminal devices, default value is 700mV, max out put is 1000mv.

### CPU Clock Skew0 :

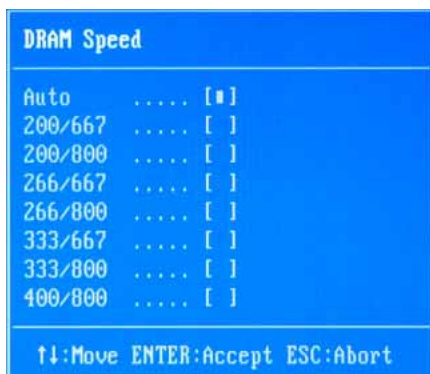
The skew of clock signal for CPU; To achieve higher FSB, please add more ps for increasing CPU OC ability. Default value is 0mV, max out put is 1500mv.

\*\*\* Recommend to add 100ps~200ps when if the FSB is higher to 450~600MHz or DRAM speed at 1800~2000MHz

### CPU Clock Skew1 :

The skew of clock signal for North-Bridge; To achieve higher FSB, please add more ps for increasing CPU OC ability. Default value is 0mV, max out put is 1500mv.

### DRAM Speed:



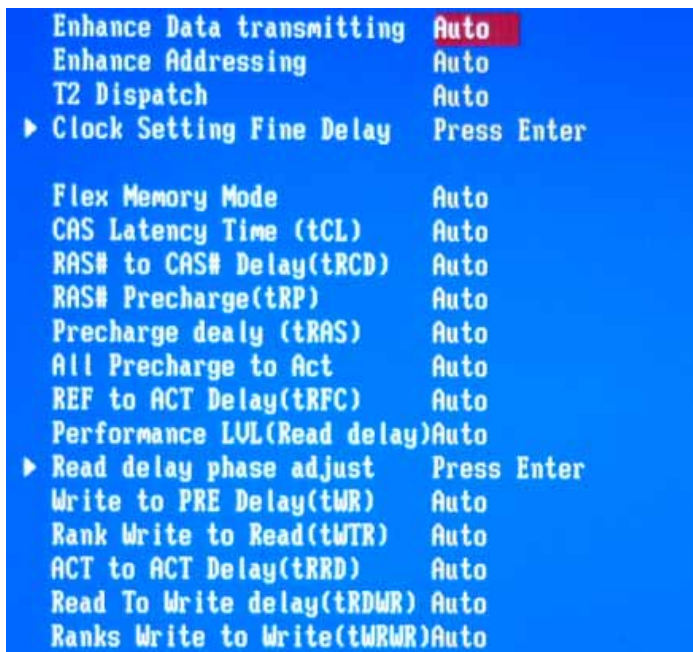
### PCIE Clock : 100MHz~250MHz

➤ CPU Feature:



(For gaining a maximum CPU utilization, we will always disable all CPU key features except “Core multi-Processing”)

➤ DRAM Timing:



**Enhance Data Transmitting: Auto / Normal / First / Turbo**

DFI specifically designed a “fine-tune mode” for DATA transmitting performance, Normal for lowest performance, Fast for highest performance, Default AUTO will automatically adjust performance based on current system Front Side BIOS.

**Enhance Addressing: Auto / Normal / First**

DFI specifically designed a “fine-tune mode” for DATA addressing, “Normal” for lowest performance, “Fast” for highest performance, Default AUTO will automatically adjust performance based on current system Front Side BIOS.

**T2 Dispatch: Auto/ Enabled / Disabled**

DRAM performance parameters patch, enabling for getting optimized and disabling to relax DRAM

timing for running higher working frequency on modules.

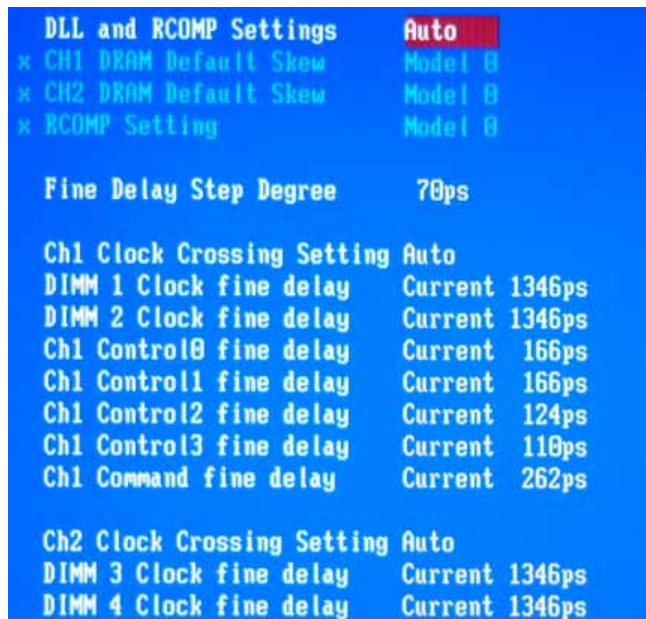
### Performance level:

It is tRD of DRAM parameter

### Read delay phase adjust:

It is the fine-tune feature for tRD

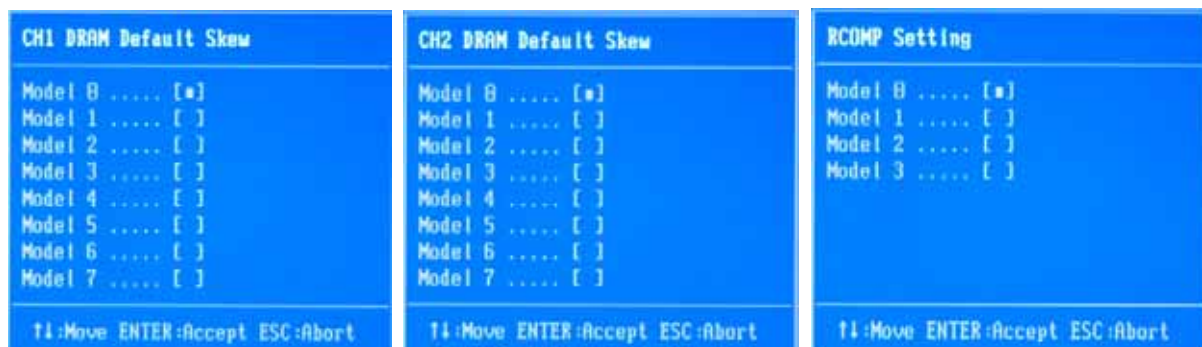
#### ➤ CLK setting fine delay:



#### DLL and RCOMP Settings: Auto/By Menu

**DRAM DLL table** is a base for calculating clock delays; they are very important parameters for control singles delivering between CPU, NB and DRAM. **Genie BIOS** has provided 7 models to make more suitable parameters for running higher DDR2 speed.

**RCOMP Values** is NB chipset register, it is impedance relating, change it will help to match signal requirement when run into a higher DRAM speed.



\*\*\* Recommend fine delay and RCOMP settings for DRAM Ratio when OC to 450~600MHZ \*\*\*

#### DRAM ration @ 333:667, 266/667

CH1/ CH2/ RCOMP Setting: **3/ 3/ 1, 5 /5 /1**

#### DRAM ration @ 400:800, 333:800,

CH1/ CH2/ RCOMP Setting: **0/ 0/ 2**

### Fine Delay Step Degree:

Scale gap from 10ps ~160ps, each scale can be able to adjust 31 degree steps.



### How to use it?

For example: if you would like to manual set 310ps for DIMM1 Clock fine delay

**Fine Delay Step Degree=10ps**

**DIMM 1 Clock Fine Delay=31 DEG**

For reaching 620ps, just need to change “Fine Delay Step Degree=20ps”

### Ch1 / Ch2 Clock Crossing Setting:

**Auto / More aggressive /aggressive / Nominal / Relaxed / More Relaxed**

Giving an easy explanation, after the CPU, PCIE, DRAM locked the clock phase by “PLL phase locked loop”, we can utilize the DRAM DLL to adjust DRAM operating phase by tuning DRAM DATA output phase forward or backward to create a better match with current DATA operating phase.

The BIOS will automatically calculate a parameter after system boot up.

The BIOS will show the current value of this parameter.

The best tuning range for finding the best DATA operating phase will be 3 ranks before or after this current value.

### Ch1Ch2 CommonClock Setting:

**Auto / More aggressive /aggressive / Nominal / Relaxed / More Relaxed**

As above, it is PLL fine-tune for Common clock signals of DRAM modules.

### Ch1/Ch2 RDCAS GNT-Chip Delay: Auto /1~7 CLK

Read command rate, 1Clock is Intel Command rate 1N mode, 2~7Clock are 1N disable mode

### Ch1/Ch2 WRCAS GNT-Chip Delay: Auto /1~7 CLK

Write command rate, 1Clock is Intel Command rate 1N mode, 2~7Clock are 1N disable mode

### Ch1/Ch2 Command to CS Delay: Auto /1~7 CLK

DRAM module bank selecting command rate, 1Clock is Intel Command rate 1N mode, 2~7Clock are 1N disable mode

### Common CMD to CS Timing”

DRAM command rate mode 1N and 2N (1N disable) selection.

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### NB Core Voltage: (1.265V~2.040V)

NB Core Voltage	NB Core Voltage
1.1825 ..... [*]	1.8825 ..... [ ]
1.1950 ..... [ ]	1.8950 ..... [ ]
1.2075 ..... [ ]	1.9075 ..... [ ]
1.2200 ..... [ ]	1.9200 ..... [ ]
1.2325 ..... [ ]	1.9325 ..... [ ]
1.2450 ..... [ ]	1.9450 ..... [ ]
1.2575 ..... [ ]	1.9575 ..... [ ]
1.2700 ..... [ ]	1.9700 ..... [*]

### CPU VTT Voltage range: (1.10V~1.60V)

CPU VTT Voltage	CPU VTT Voltage	CPU VTT Voltage
1.10 ..... [*]	1.23 ..... [ ]	1.53 ..... [ ]
1.11 ..... [ ]	1.24 ..... [ ]	1.54 ..... [ ]
1.12 ..... [ ]	1.25 ..... [ ]	1.55 ..... [ ]
1.13 ..... [ ]	1.26 ..... [ ]	1.56 ..... [ ]
1.14 ..... [ ]	1.27 ..... [ ]	1.57 ..... [ ]
1.15 ..... [ ]	1.28 ..... [ ]	1.58 ..... [ ]
1.16 ..... [ ]	1.29 ..... [ ]	1.59 ..... [ ]
1.17 ..... [ ]	1.30 ..... [*]	1.60 ..... [*]

### Vcore drop control: Enable / Disabled

Enabling to control Vout level by PWM, disabling to get a maximum output.

### Clockgen voltage control: (3.45V~3.85V)

Clock working voltage, increase it to achieve higher and more stable in extreme FSB environment

### GTL+ buffer Strength: Strong / Weak

It is adjustment option for North-Bridge reference voltage strength.

### Host Slew Rate: Strong / Weak

It is adjustment option for North-Bridge voltage driving strength.

### GTL REF Voltage control: Enable / Disabled

CPU VTT reference voltage for determining host bus high / low level.

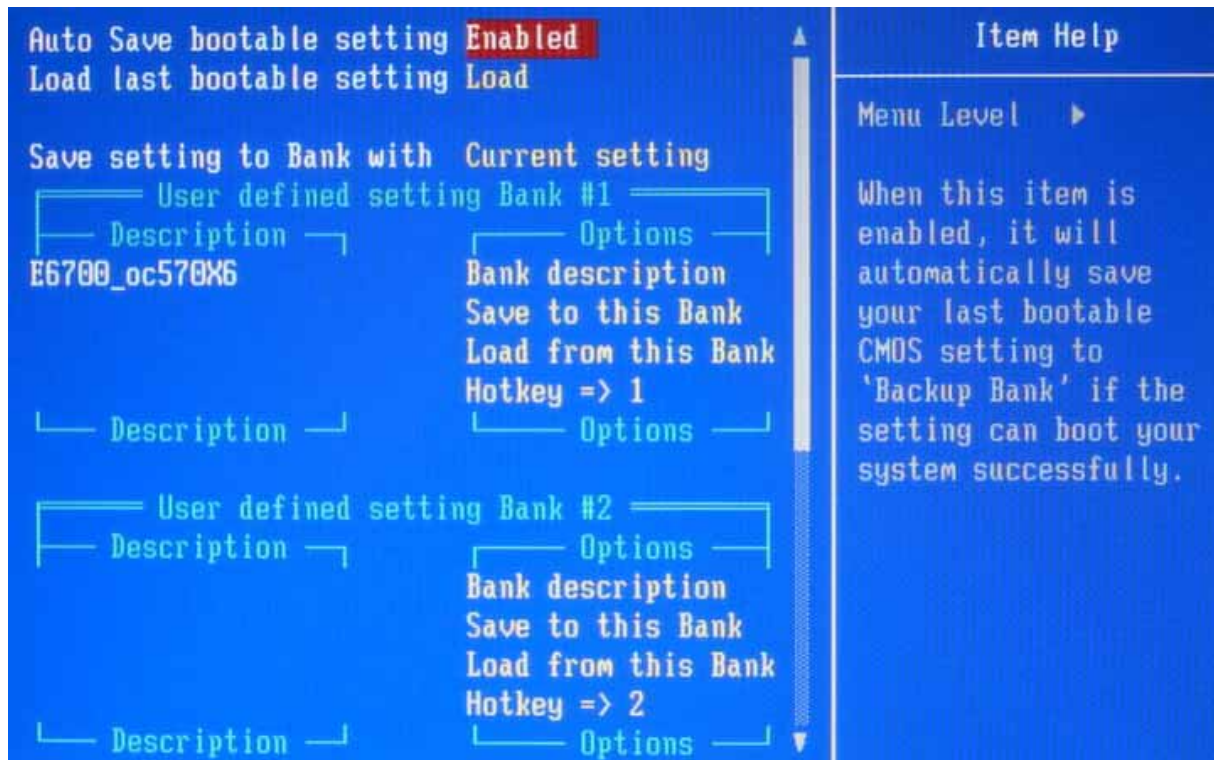
### FSB REF: AUTO

MCH parameter registers for reaching highest FSB. Some of CPU can broken FSB wall after modified following values.

\*\*\* Recommend settings \*\*\*

Value: AUTO /23 /24 /26

- BIOS Reloaded function: *DFI Lan Party series are providing 1last fine status + 4 user's profile space for doing BIOS setting saving and recovery.*



**Auto Save bootable setting:** Enable / Disable

For saving last fine/ bootable parameters by BIOS itself every time

**Load last bootable:**

For loading last BIOS parameters.

**Save setting to bank with:** Current settings or last saved CMOS settings.

To define the resource of parameters for bank saving.

**User define setting bank #1 ~ #4:**

1. **Bank Description:** There are 4 rows for writing a short description. Double click on row when this row is empty, it will erase pervious data.



2. **Save to this bank:** Press "Y" to save data to this bank
3. **Load from this bank:** Press "Y" to load data of this bank to be current BIOS setup settings.
4. **Hotkey =>:** define the "hotkey" for quick change BIOS settings to boot. Please press Hotkey after power on system immediately.

➤ EZ Clear CMOS methods:

a. **EZ clear jumper**

b. To **hold Home key** to power on system, BIOS will recover FSB to default, remains setting will be keeping the last time fine status.



c. To **hold Insert key** to power on system, BIOS will load all setting back to default as like doing a CCMOS by manually.



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End